Electric Mobility

"ecoCity eMotion"

24-25th September 2014, Erlangen, Germany

Eniac IDEAS contribution to electromobility

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Introduction

The goal of
Eniac IDEAS *"Interactive Power Devices for Efficiency in Automotive with Increased Reliability and Safety"*

is to develop

- advanced packaging for power supply components and
- new generation memory systems having application on Electric and ICE propelled vehicles

and thus to complement running ENIAC and ARTEMIS Automotive projects. Project entered its final Y3 period and offers already tangible outcomes for EV producers.

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Presentation Outline

- IDEAS consortium
- Tangible outcomes beyond the state-of-the-art
- Complementary activities
  (Cross fertilization of IDEAS achievements)

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IDEAS Consortium

Partner	Beneficiary name	Short name	Country
1	STMICROELECTRONICS SRL	ST-I	IT
2	CRF -withdrawn		
3	Bitron	BIT	IT
4	Micron Semiconductors Italia	MIY	IT
5	Poli Model srl	POLIM	IT
6	Politecnico di Torino .	POLITO	IT
7	University of Perugia	UniPG	IT
8	University of Roma	UniRM	IT
9	Institut mikroelektronických aplikací s.r.o .	IMA	CZ
10	Institute of Information Theory and Automation	UTIA	CZ
11	Brno University of Technology .	BUT	CZ
12	Warsaw University of Technology	WUT	POL
13	AUTOMOTIVE Industry Institute	PIMOT	POL
14	DEST	DEST	POL
15	ISD	ISD	GRE

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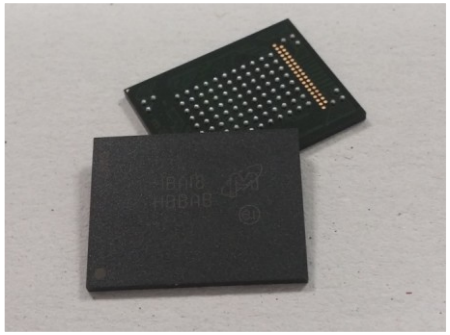
Tangible outcomes beyond the state-of-the art

(1) High reliability **eMMC device** for Driving Assistance (Micron)



IDEAS R&D topic	State-of-the-Art	Innovation	Goals
High safety eMMC device for Driving Assistance (MIY)	Operative temperature range: -25dC / +85dC	Operative temperature range: -40dC / +85dC	Operative temperature range: -40dC /+105C
	Limited power loss immunity	Full power loss immunity	Full power loss immunity (confirmed)
	Failure rate: <500ppm	Failure rate: <50ppm	Failure rate: <20ppm
	Lifetime: 5years	Lifetime: 15years	Lifetime: 15years (confirmed)
	Standard package BGA 0.5mm pitch	Reliable package BGA 1mm pitch, with test-pads	Reliable package BGA 1mm pitch, with test-pads (confirmed)
	JEDEC 4.51 specs	JEDEC 4.51 specs	JEDEC 5.0 specs on 128GB density

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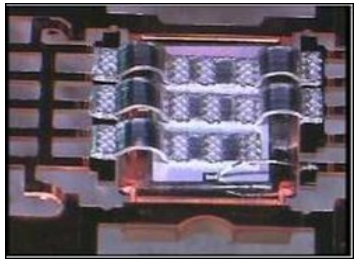
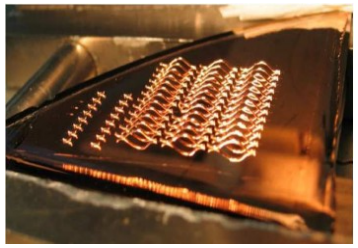
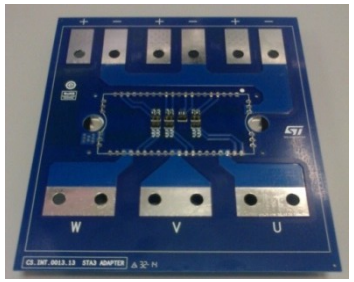
Figure: Wafer sorting in clean room (Micron)

Tangible outcomes beyond the state-of-the art

(2) **Ag sintering trials, Al ribbon Cu copper wires trials** (ST-I)







Interconnection technologies (ST-I)	Today's manufacturing of heavy wire bonding is done with Al wires on Al/Si front metal	Heavy Cu bonding on Cu front metal	To drastically improve the reliability performances vs. thermal and power cycles (up to 10X life time). Additional RDS(on) reduction by >10% thanks to better Cu conductivity
Advanced die attach (ST-I)	Soft solder or preform die attach	Ag powder material in sintering process	Power Leadfree manufacturing achieves higher productivity by dispensing on substrate. This is expected to improve thermal and electric conductivity up to 2X vs. standard die attach.
	Soft solder or preform die attach	Ag sintering process	The Ag sintering material permits the joint to have operative temperature much higher than standard solder materials. Due to the higher melting temperature (961°C) there are better performances on thermo mechanical fatigue.
	Soft solder or preform die attach	Ag sintering process	To improve yield by 3% and global quality. To drastically improve the reliability performances vs. thermal and power cycles (up to 10X life time).
Device (ST-I)	Si die	SiC MOSFET	Increase device efficiency
	Si die	SiC MOSFET	Increase operative temperature Tj up to 200°C (current case standard is 125°C)

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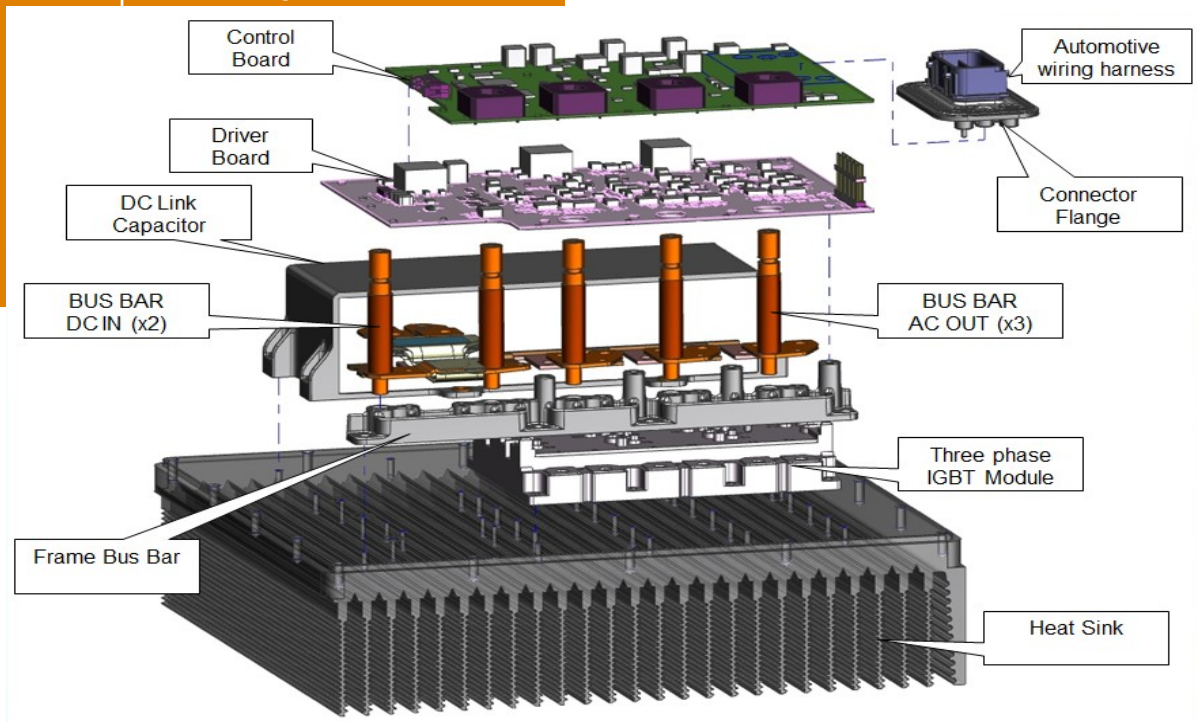
Tangible outcomes beyond the state-of-the art

EV DC fast charging system (BIT)	**All around the world most of the EV charging systems installed on the road network are based on AC architecture. Car-makers required the introduction of DC architecture in order to reduce the time needed for EV battery charging and delete the on board AC-DC converter interfaced to Battery Management System.**	**Realization of a DC converter with Si IGBT technology for EV DC fast charging, as requested by European and Japanese car-makers**	• **A demonstrator was realized with Si IGBT technology whose efficiency is up to 94.5%** • **Demonstrator is compliant to CHAdeMO standard, used by Japanese car-makers** • **Demonstrator is compliant to COMBO standard, used by European car-makers**

(3) Silicon IGBT converter for fast vehicle charging, able to supply up to 50kW from 50 to 500V



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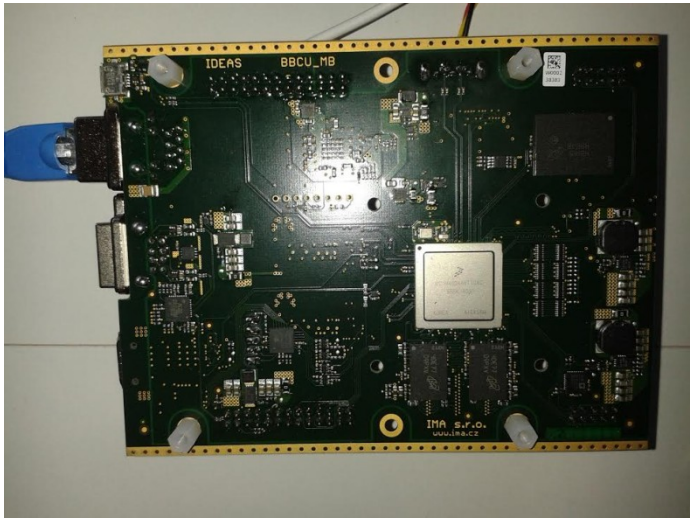
Tangible outcomes beyond the state-of-the art

(4) Body and Board Control Unit (IMA)



Body and Board Control Unit BBCU (IMA)	**ECU units became essential part of vehicle security system, their interfaces and busses allow both passengers and vehicle high comfort and reliability. ECUs take care of engine control, brakes, driver assistance as well as car entertainment and comfort. Recent ECUs improve the traffic safety providing emergency information in case accident (e.g. emergency call when air bags are activated).** **Todays, no unit is capable to store high amount of the data flowing from the sensors, cameras and moreover to transfer them outside from the vehicle. Attempts are made with dedicated devices supporting eCALL function.**	**Future safety policy in always heavier traffic will require additional data to solve more efficiently car accidents (similarly to airplane black box) and support traffic fluency (e.g. on line and on time data about traffic density, car failure). The reliable storage system should secure sensitive data even in case of heavy car mechanical damage.**	**The BBCU is a new vehicle unit designed in order to meet above functionalities and act as fly recorder. BBCU design integrates new high reliable Micron memories; GPS, 3G and video interfaces.** **Parameters:** **i.MX6 dual core automotive MCU 1GHz, 2GB RAM, 32GB automotive e.MMC memory** **2x CAN, Ethernet, UART.** **Power management and battery to record and communicate even without external power supply. Durable case.** **One separable memory for better protection and for better access after accident.**

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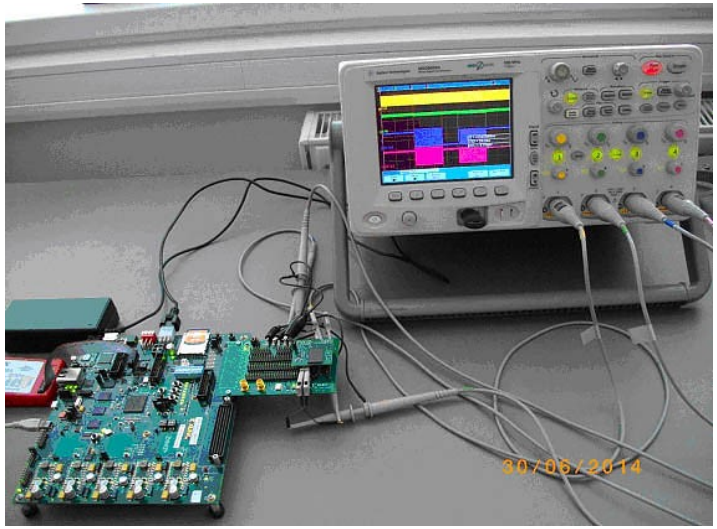
Tangible outcomes beyond the state-of-the art

(5) Memory testing platform
(UTIA)



Memory testing platform (UTIA)	**Various memory testing tools exists. They are usually focused to specific application or requested results and usually cover only limited range of memory testing problematic.**	**Set of testing tools which cover all levels of memory testing problematic; Precise FPGA based testing tool for lower level memory communication testing;** **Higher level testing tools available for two major OS used in embedded systems (Linux and Microsoft Windows CE)**	• **Develop ARM based generic HW platform for memory testing** • **Develop FPGA based HW tool for memory communication testing** • **Prepare SW tools for both ARM and FPGA**
DDR3 memory interfaces architecture for FPGA SoC designs	FPGA SoC Xilinx Zynq with ARM A9: DDR3 666 MHz clock 32 bit	Designed FPGA SoC (KC705 board, Kintex 28nm) AXI4 interconnect 128 bit. DDR3 800 MHz clock 64 bit = 2.4x increased DDR3 bandwidth	• High DDR3 bandwidth to store sequences of HDMI resolution video data frames in FPGA design.
Video Sensor interfaces to FPGA	1x 1920x1080p60 (Zynq with ARM A9)	2x 1920x1080p60 KC705 board, Kintex FPGA, 28nm)	Capability to process or store to DDR3 multiple HD video stream sequences in real time
Embedded floating point computations in FPGA	FPGA SoC designs: MicroBlaze 150 MHz with HW FP (KC705 board, Kintex 28nm) 10 MFLOPS@2W (200mW/MFLOPS)	FPGA SoC designs: MicroBlaze 150 MHz with HW FP (KC705 board, Kintex 28nm) with Single 8xSIMD EdkDSP accelerator 2400MFLOPS@3W (1.25mW/MFLOP)	• Reduction of power per MFLOPS by use of floating point accelerators for computations in the FPGA based Active Driver Assistance designs.

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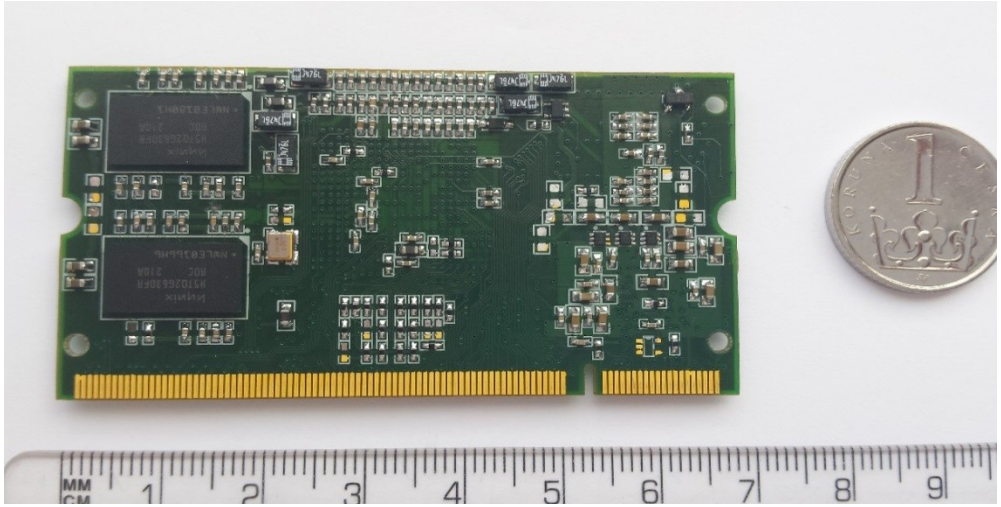
Tangible outcomes beyond the state-of-the art

(6) Processor module – ARM based SoM with eMMC
(BUT)



Processor module – ARM based SoM with eMMC (BUT)	**SoM - System on Modules are equipped either by a NAND Flash or eMMC memory as non-volatile memory for data storage. SoM with eMMC needs another non-volatile memory as a boot memory.**	**ARM based SoM with eMMC memory will use this memory as a data storage and also as a boot without necessity to use another non-volatile memory. This innovation can reduce complexity and make OS boot process faster.**	• **Develop ARM based SoM with eMMC as a boot and data storage memory.** • **Modify OS BSP to support eMMC as a boot memory.**

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Complementary activities

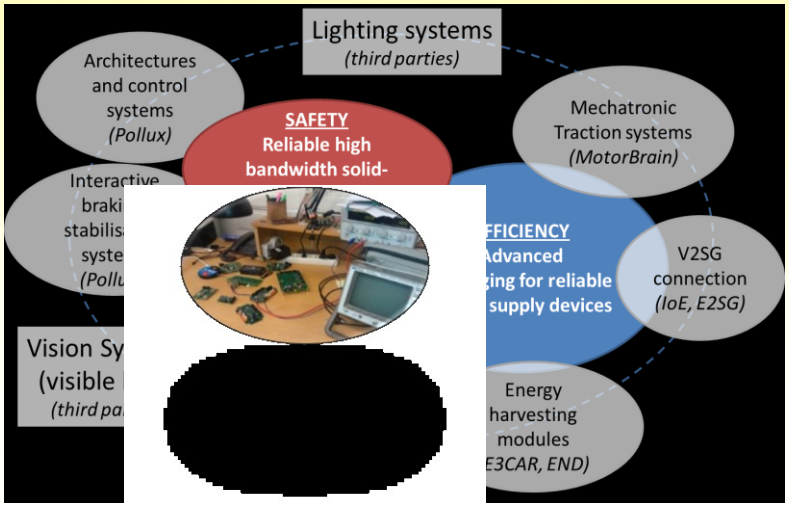
SysDes

EM-IEM
ElectroMagnetic Reliability of Electronic Systems for Electro Mobility

MOTOR BRAIN

IoE
Internet of Energy

3CAR



EMC²

CC Cyber City

Adaptive Cooperative Control in Urban (sub) Systems
ACCUS

GUARD

TSComConE

Passionate

UPTOWN

Thank you for your attention

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